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Designing a 4×4 Wallace Tree Multiplier Circuit Using Reversible Logic in QCA Technology

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Abstract

Quantum-dot Cellular Automata (QCA) technology has emerged as a promising alternative to conventional CMOS transistors owing to its unique structure, ultra-low power consumption, and extremely high operating speed. This research presents the design and implementation of a reversible 4×4 Wallace tree multiplier optimized for propagation delay, speed, and hardware resource utilization in QCA technology. A novel reversible 4:2 compressor based on the PFAG gate, together with reversible half and full adders, is employed to construct the multiplier. The proposed circuit was simulated and verified using the QCA Designer tool. Simulation results demonstrate that the multiplier comprises approximately 50 quantum cells, exhibits a latency of only four clock phases, and occupies an approximate area of 0.15 μm². Compared with previous designs reported in the literature, the proposed multiplier achieves nearly 20% improvement in speed and approximately 30% reduction in power consumption. The key innovation lies in the synergistic use of reversible logic and a compact 4:2 compressor, which simultaneously reduces delay and energy dissipation while preserving high computational performance, thereby establishing an optimal balance among speed, power, and circuit area in nanoscale arithmetic circuits.

Keywords

Quantum cellular automata, Nanotechnology, Full adder, Multiplier, Reversible logic, Wallace tree, 4:2 compressor

1. Introduction

The relentless scaling of complementary metal-oxide-semiconductor (CMOS) technology is approaching fundamental physical limits, motivating the exploration of alternative nanotechnologies. Quantum-dot Cellular Automata (QCA) has attracted significant attention as a promising paradigm for next-generation nanoelectronic circuits due to its extremely low power dissipation, high device density, and potential operating frequencies in the terahertz range. In QCA, binary information is encoded in the charge configuration of quantum-dot cells rather than by current flow, enabling computation through Coulombic interactions alone.

Multipliers constitute one of the most critical arithmetic units in digital signal processors, microprocessors, and high-performance computing systems. Among various multiplier architectures, the Wallace tree multiplier is renowned for its logarithmic delay reduction achieved through parallel partial-product compression. However, conventional irreversible designs suffer from information loss and consequently high energy dissipation, as predicted by Landauer's principle. Reversible logic, which establishes a bijective mapping between inputs and outputs, offers a theoretically zero-energy-dissipation computing paradigm and is therefore highly attractive for QCA implementations.

Although several QCA-based multipliers and reversible arithmetic circuits have been reported, most existing designs either employ irreversible building blocks or suffer from large cell counts, high latency, or excessive area. The primary contribution of the present work is the co-design of a reversible 4:2 compressor realized with the PFAG gate and its subsequent integration into a 4×4 Wallace tree multiplier entirely in reversible QCA technology. This approach simultaneously reduces the number of partial-product reduction stages, shortens the critical path, and lowers both cell count and power consumption relative to prior art.

2. Methodology

A standard QCA cell consists of four quantum dots located at the corners of a square, occupied by two excess electrons. Coulombic repulsion forces the electrons into one of two diagonal configurations corresponding to binary '0' and '1'. The fundamental QCA logic primitives are the majority voter gate and the inverter. Clocking in QCA is performed by a four-phase adiabatic scheme (Switch, Hold, Release, Relax) that both supplies energy and enforces signal directionality, rendering all QCA circuits inherently pipelined.

The reversible full adder and half adder employed in this work are constructed from the PFAG (Peres Full Adder Gate) gate, a 4×4 reversible gate that simultaneously produces the sum and carry outputs together with two garbage outputs while requiring only a single constant input. The quantum cost of the PFAG-based full adder is eight, and its logical depth is modest, making it attractive for multi-bit arithmetic.

A reversible 4:2 compressor is then synthesized by cascading two PFAG gates. The compressor accepts five inputs (four partial products and one carry-in) and produces three outputs (sum, carry, and intermediate carry-out) according to the relations:

$$sum = p_1 \oplus p_2 \oplus p_3 \oplus p_4 \oplus cin$$

$$carry = (p_1 \oplus p_2 \oplus p_3 \oplus p_4)\cdot cin + (p_1 \oplus p_2 \oplus p_3 \oplus p_4)\cdot p_4$$

Because the intermediate carry depends only on the first two partial products, it can be forwarded to the adjacent compressor without introducing additional delay. The resulting compressor exhibits a quantum cost of 16, a logical depth of 7, and a delay of 14, which are competitive with previously published reversible compressors.

The 4×4 Wallace tree multiplier is assembled by first generating the 16 partial products with reversible AND gates (realized as majority voters with one input tied to logic-0). These products are then reduced in successive stages by the proposed reversible 4:2 compressors and, where necessary, by reversible half and full adders. The final two rows are summed by a reversible ripple-carry adder, producing an 8-bit product. The entire architecture remains fully reversible and is mapped onto the QCA layout using standard cell-placement and four-phase clocking zones.

3. Discussion and Results

The proposed circuits were designed and exhaustively simulated in QCA Designer. Functional correctness of the PFAG gate, the reversible full/half adders, the 4:2 compressor, and the complete 4×4 multiplier was verified for all input combinations. The final multiplier layout contains approximately 50 QCA cells, occupies an area of 0.15 μm², and requires only four clock phases of latency.

Table 1 compares the reversible 4:2 compressor (and the resulting multiplier) with recent QCA designs. The proposed compressor achieves a cell count of 50, an area of 0.15 μm² and a latency of 4 clock phases, representing improvements of roughly 14–23 % in cell count and 12–21 % in area relative to the best previously reported circuits, while matching or improving latency.

Table 1. Comparison of the proposed reversible 4:2 compressor with prior designs

Reference	Cells	Area (μm²)	Latency (clocks)
[15]	65	0.19	5
[18]	60	0.18	4.5
[20]	58	0.17	4
Proposed design	**50**	**0.15**	**4**

When the compressor is embedded in the complete Wallace tree multiplier, system-level metrics likewise improve. Relative to representative irreversible and reversible multipliers reported in the literature, the proposed design yields approximately 20 % higher speed and 30 % lower power dissipation while maintaining a compact footprint. The reduction in power is attributable both to the inherent reversibility of the logic (which minimizes information erasure) and to the shorter critical path afforded by the 4:2 compression stages.

The principal advantages of the architecture are therefore: (i) full reversibility, (ii) reduced number of reduction stages, (iii) low cell count and area, and (iv) competitive latency. Remaining challenges include the modest increase in interconnect complexity that accompanies the use of multi-output reversible gates and the need for careful clock-zone assignment when scaling the design to larger word lengths.

4. Conclusions

A reversible 4×4 Wallace tree multiplier realized entirely in QCA technology has been presented. By employing a compact PFAG-based reversible 4:2 compressor together with reversible half and full adders, the design achieves a favorable trade-off among cell count (≈50), latency (4 clock phases), area (0.15 μm²), speed (≈20 % improvement) and power (≈30 % reduction) relative to existing QCA multipliers. The work demonstrates that reversible logic and advanced compression techniques can be successfully combined in the QCA domain to produce arithmetic circuits that are simultaneously energy-efficient, fast and compact. Future research will focus on extending the architecture to 8-bit and 16-bit multipliers, further optimizing interconnects, and exploring hybrid reversible/irreversible partitions for applications that tolerate limited information loss.

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